Lithography Strategy for 65nm Node

Y. Borodovsky, R. Schenker, G. Allen, E. Tejnil, D. Hwang, F. C. Lo, V. Singh, R. Gleason, J. Brandenburg, R. Bigwood

Logic Technology Development, Technology and Manufacturing Group, Intel Corp.
RA1-240, 5200 NE Elam Young Parkway, Hillsboro, OR 97124-6497
Phone 503-613-6079, FAX 503-613-7013, email: yan.borodovsky@intel.com

Introduction

Intel will start high volume manufacturing (HVM) of the 65nm node in 2005. Microprocessor density and performance trends will continue to follow Moore's law and cost-effective patterning solutions capable of supporting it have to be found, demonstrated and developed during 2002-2004. Given the uncertainty regarding the readiness and respective capabilities of 157nm and 193nm lithography to support 65nm technology requirements, Intel is developing both lithographic options and corresponding infrastructure with the intent to use both options in manufacturing.

Development and use of dual lithographic options for a given technology node in manufacturing is not a new paradigm for Intel: whenever introduction of a new exposure wavelength presented excessive risk to the manufacturing schedule, Intel developed parallel patterning approaches in time for the manufacturing ramp. Both I-line and 248nm patterning solutions were developed and successfully used in manufacturing of the 350nm node at Intel. Similarly, 248nm and 193nm patterning solutions were fully developed for 130nm node high volume manufacturing.

65nm Node Patterning Evolutionary Path.

Moore's law manifests itself through inter-generational doubling of IC density (**Figure 1**). Following the established trend (**Figure 2**), it is apparent that 65nm node density requirements necessitate patterning support for 0.5 μm^2 area SRAM bit cell. Scaling the 1.0 μm^2 area of Intel's existing 90nm node bit cell [1] by 50% implies that robust 160nm pitch patterning capabilities will be required for 65nm node logic integrated circuit (IC) manufacturing. Given the projected tooling and materials availability in 2003-2005 and the specifics of Intel product lines and manufacturing costs, only optical 157nm and 193nm approaches are considered to be suitable for patterning of 65nm node critical layers in HVM at Intel. Data in **Figure 3** show growth in the manufacturing complexity as represented through inter-generational change in the Rayleigh k_1 factor for patterning approaches already developed in support of Intel products as well as for approaches needed in support of 65nm technology node.

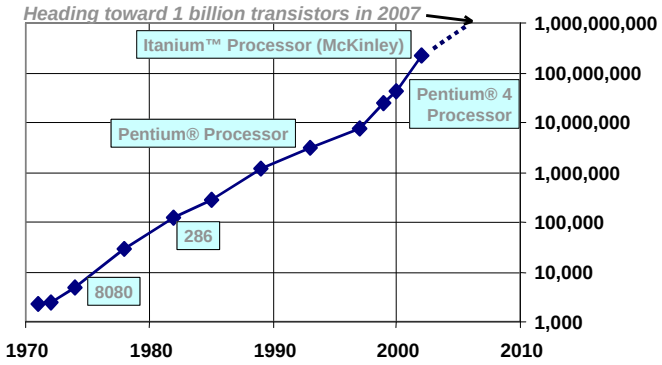

Figure 1. Illustration of Moore's Law – transistor count for Intel products as a function of time.

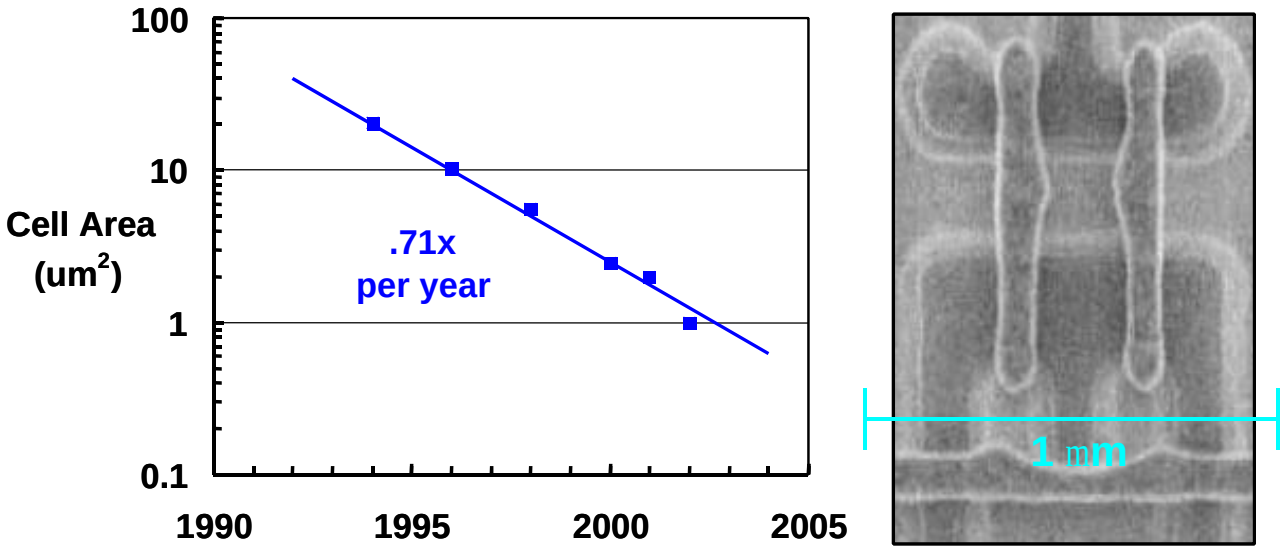

Figure 2. (Left) Intel SRAM Bit Cell area evolution versus time. (Right) 1 micron square bitcell.

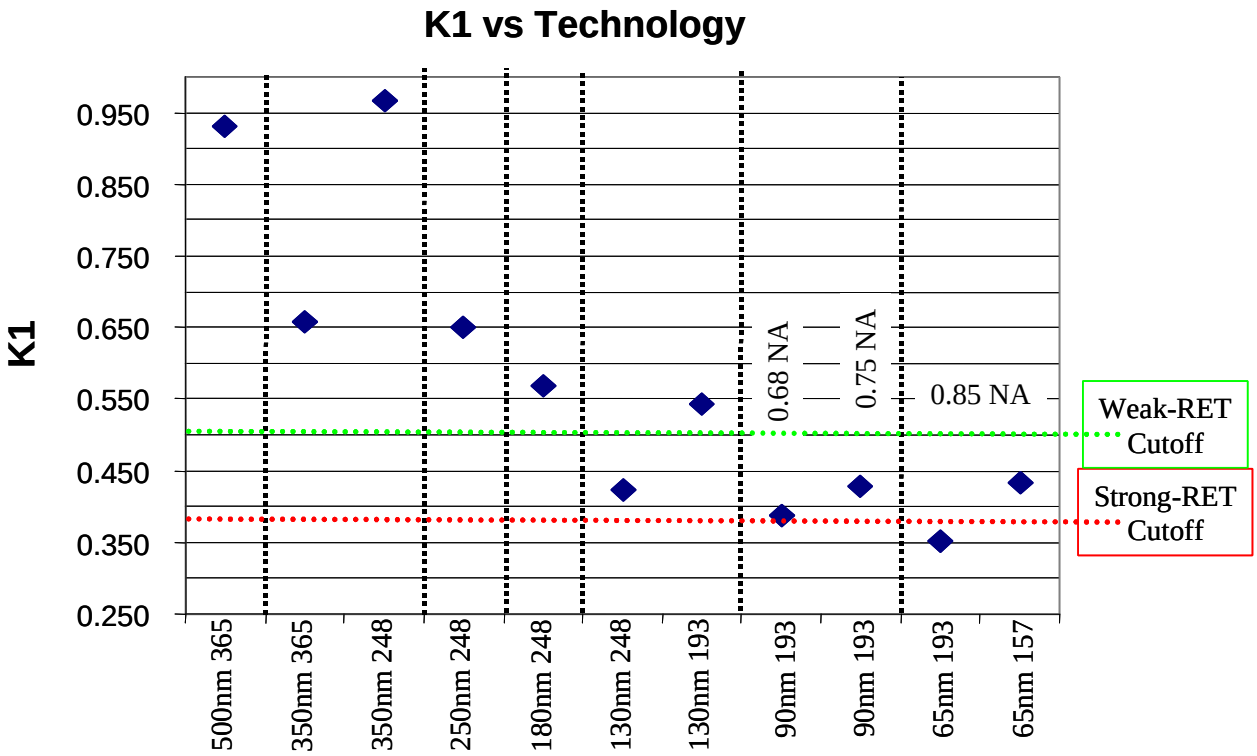

Figure 3. Generation dependence of k_1.

Steady decline in k_1 led to development and wide use in manufacturing of "weak" resolution enhancement techniques (RET) including off-axis illumination, attenuated phase shift masks (PSM), various assist features implementation schemes and a massive increase in use and complexity of optical proximity correction (OPC). Lower k_1 patterning was further enabled by immense progress in resist capabilities as judged by "NILS Capable" resist performance (**Figure 4**), unprecedented improvements in exposure tools aberrations control, and introduction of design rules restrictions

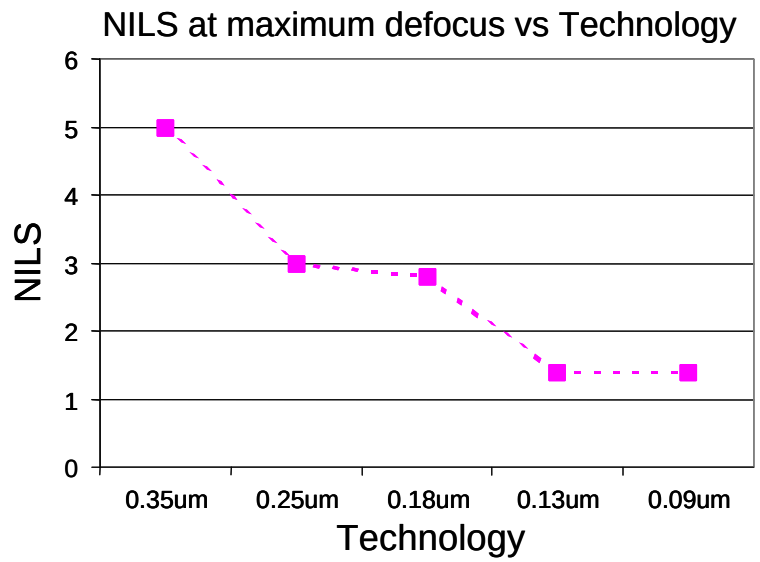

Figure 4. Trend of resist NILS vs Technology. NILS are for 1/1 line/space pattern at tightest pitch and at maximum allowed defocus for that generation.

necessary to support RET + OPC. This in turn placed massive pressure on mask making infrastructure to develop and sustain cost effective processes capable of producing wide variety of zero defect masks to ever decreasing values of dimensional control for mask databases that grew in size on average by more than 2.5X per year (**Figure 5**) over the last decade. Evolutionary character of these multiple developments over last decade, their inter-generational re-use and incremental introduction allowed for creation of powerful and cost effective tooling, materials and patterning solutions that fueled the unprecedented rate of industry growth over those years.

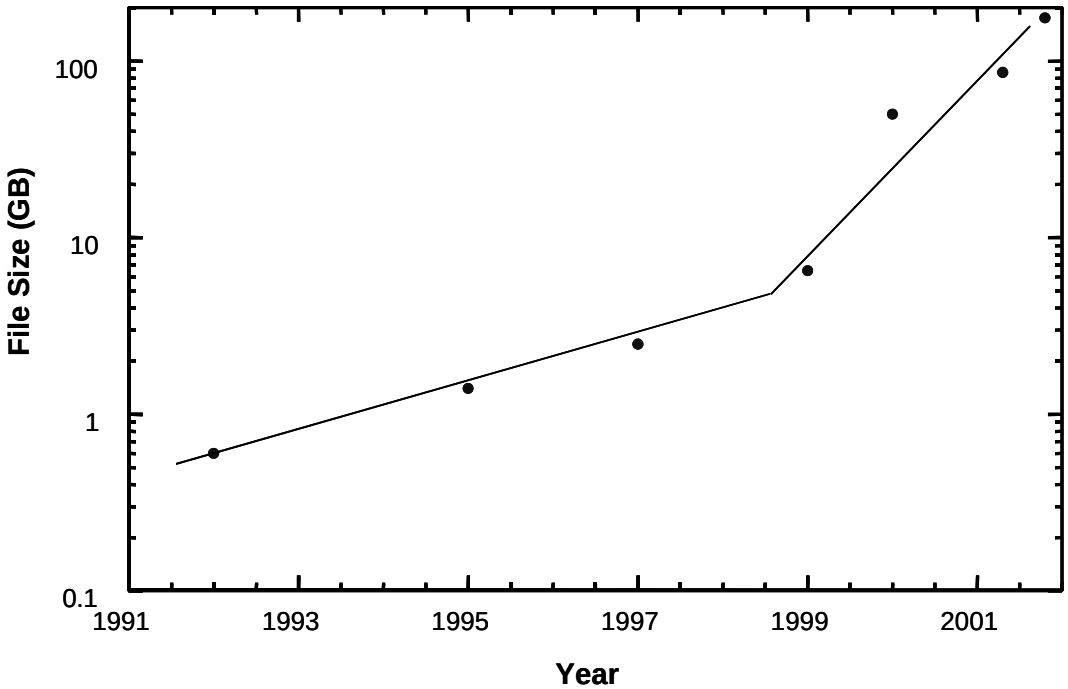

Figure 5. Increase in sizes of full-product pattern data files due to increasing transistor count, more complex OPC and proliferation of OPC through additional masking layers.

As implied in **Figure 3**, patterning solutions for 160nm pitch with the use of 157nm lithography will be similar to those used in 248nm-based manufacturing for 130nm node and already demonstrated in development for 193nm-based 90nm technology node at k1 ≥0.4. Use of 193nm, on the other hand, will require use of "strong" RET capable to support patterning at k_1=0.35. Either approach has its particular risks to mitigate in order to support 2005 HVM.

157nm Lithography.

There are numerous potential advantages for the use of 157nm lithography over 193nm lithography in support of 65nm node. First and foremost, 157nm lithography provides opportunities for re-use of well-established, cost effective and relatively simple patterning techniques, such as use of single exposure binary or EPSM masks, to pattern the tight-pitch layers of the 65nm node at k_1= 0.43. Due to the critical reliance of advanced patterning solutions on aggressive OPC, use of 157nm for 65nm node patterning promises to pose relatively lesser challenges to mask making than the 193nm patterning route. The extreme CD control requirements for 35nm gate patterning required for the 65nm technology node pose unique challenges. As existing line trimming techniques might not be extendable for the 65nm node, using shorter wavelength lithography has the advantage of better patterning of 65nm node generation gates to final size in resist. Furthermore, the cost of patterning layers at k_1=0.43 is about 60% less than that for k_1=0.35 due to the considerable savings associated with single layer exposures and lower mask making costs (**Figure 6**).

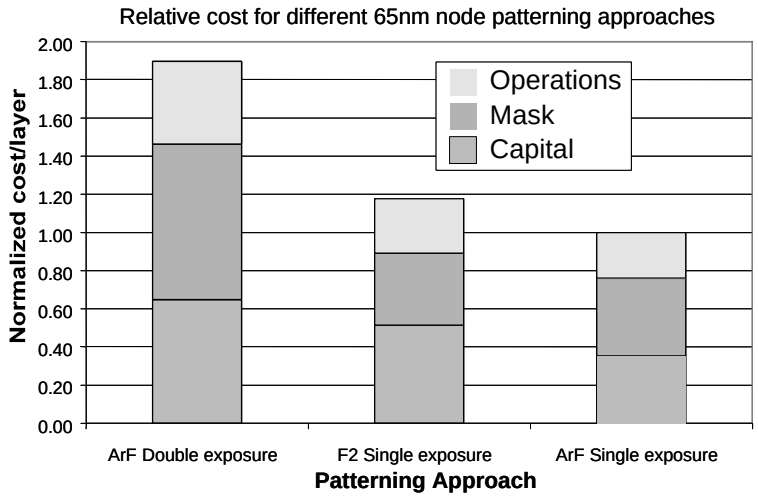

Figure 6. Illustration of relative cost per critical layer for various 65nm node patterning approaches.

A groundwork for the introduction of 157nm Lithography has been provided by the significant advances in manufacturing of F_2 laser sources, fused silica based reticle blanks, EPSM reticle blanks, and fluorine polymers based single layer resists. Additionally, the resolution of lens design issues associated with CaF_2 birefringence, the demonstration of system purging and contamination control, and the investment by the industry in CaF_2 capacity and quality control has provided a solid basis for introduction of 157nm Lithography in the near future.

The remaining mask-making challenge involving 157nm patterning is resolution of the particle protection issue in time for 157nm technology insertion into 65nm HVM. Several suppliers made great progress in synthesizing polymers and manufacturing actual pellicles with required transmission, but the durability of these materials is far from meeting requirements [2,3]. Providing traditional particle protection solution to the industry in time for 65nm HVM will require significant efforts in the understanding of soft pellicle photo-induced darkening mechanism and resolution of vacuum ultraviolet (VUV) radiation hardness issues during the next 2 years. Clearly, soft pellicle is a preferred approach for particle protection. Because concerns regarding insufficient VUV durability grew during 2001, additional efforts were put in place to develop what is known as a "hard" pellicle as a risk mitigation measure. Intel currently supports and actively participates in the development of both approaches.

Currently the projected timing of volume manufacturing of 157nm exposure tools is behind Intel's schedule for the early phase of 65nm node HVM. As a result, Intel's plan for the insertion of 157nm lithography into 65nm node manufacturing assumes the need for the later insertion of 157nm lithography with corresponding design rules provisions that will enable such insertion. Intel is working actively with multiple tooling and materials suppliers, numerous research institutions and

international consortia to ensure that the opportunity to use 157nm for 65nm node manufacturing will not be missed.

193nm Lithography.

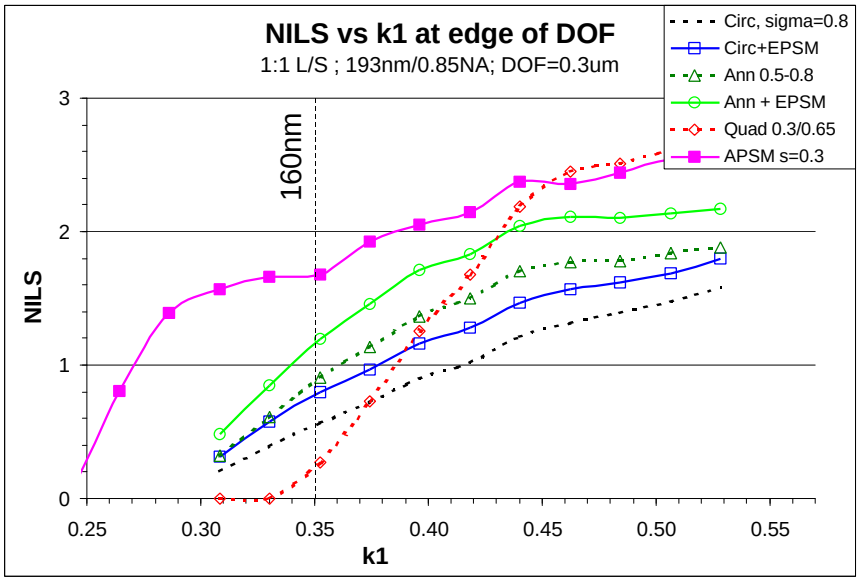

Figure 7. NILS at maximum allowed defocus level as a function of k_1 for patterning techniques applied to 1-to-1 lines and spaces.

Lithography for the 65nm node based on 193nm exposures will require patterning at k_1=0.35 to meet 160nm pitch requirements as well as inventive approaches to pattern 35nm gates with the required dimensional control. Alternating phase shift masks (AltPSM) and dual exposure patterning techniques are needed for k_1=0.35 patterning unless resists performing at normalized image log slope (NILS) of less than 1.2 can be developed (**Figure 7**). At this time, there are no demonstrated AltPSM methods that can be applied to support patterning of random logic without severe layout restrictions or at the expense of reduced pattern density. Application of AltPSM at k_1=0.35, even to restricted parts of the layout, such as microprocessor cache, requires further development of phase assignment techniques and extremely accurate predictive AltPSM and OPC modeling for double exposures. Use of AltPSM at k_1=0.35 presents unusual challenges in finding appropriate OPC solutions as the mask error enhancement factors (MEEF) can vary from <0.3 to >5.0 on various critical layers (**Figure 8**). Intel has developed the required tooling and methodology for such patterning. Both contact and metal layers for traditional SRAM 6T cells layouts were patterned using AltPSM at k_1=0.35 with 193nm with depth of focus (DOF) equal or exceeding 0.40µm.

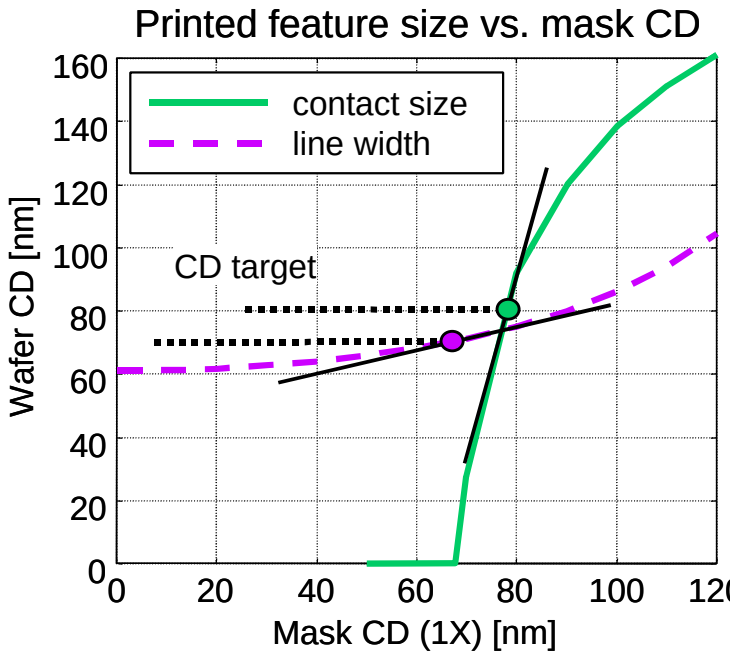

Figure 8. Simulated wafer CD versus mask CD for Alt-PSM features printing 160nm pitch using 193nm and 0.85 numerical aperture. The MEEF is the slope of the line at the CD target

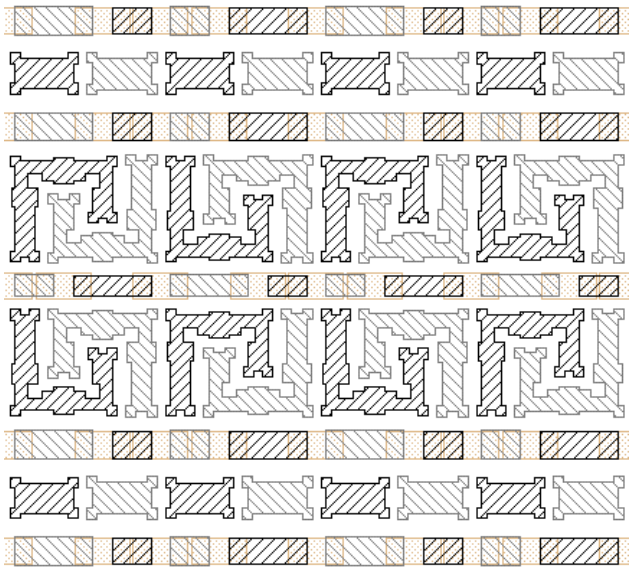

Figure 9 shows an example of phase assignment for the metal layer of a traditional SRAM layout with its corresponding wafer pattern. Despite the simplified OPC, deviations from the desired pattern are not large. **Figure 10** shows the behavior of the referred printed pattern at k_1=0.35 through PSM and trim mask focus using 193nm tooling and resist; a reasonable focus window is achieved. The dose sensitivity achieved with this layout is especially robust as shown in **Figure 11** where over-exposure of the PSM dose by 13% does not induce bridging.

Figure 9. Phase assignment and OPC for SRAM metal layer. Cross hatched regions are zero and 180 degree phase regions while dotted regions are clear regions on trim mask.

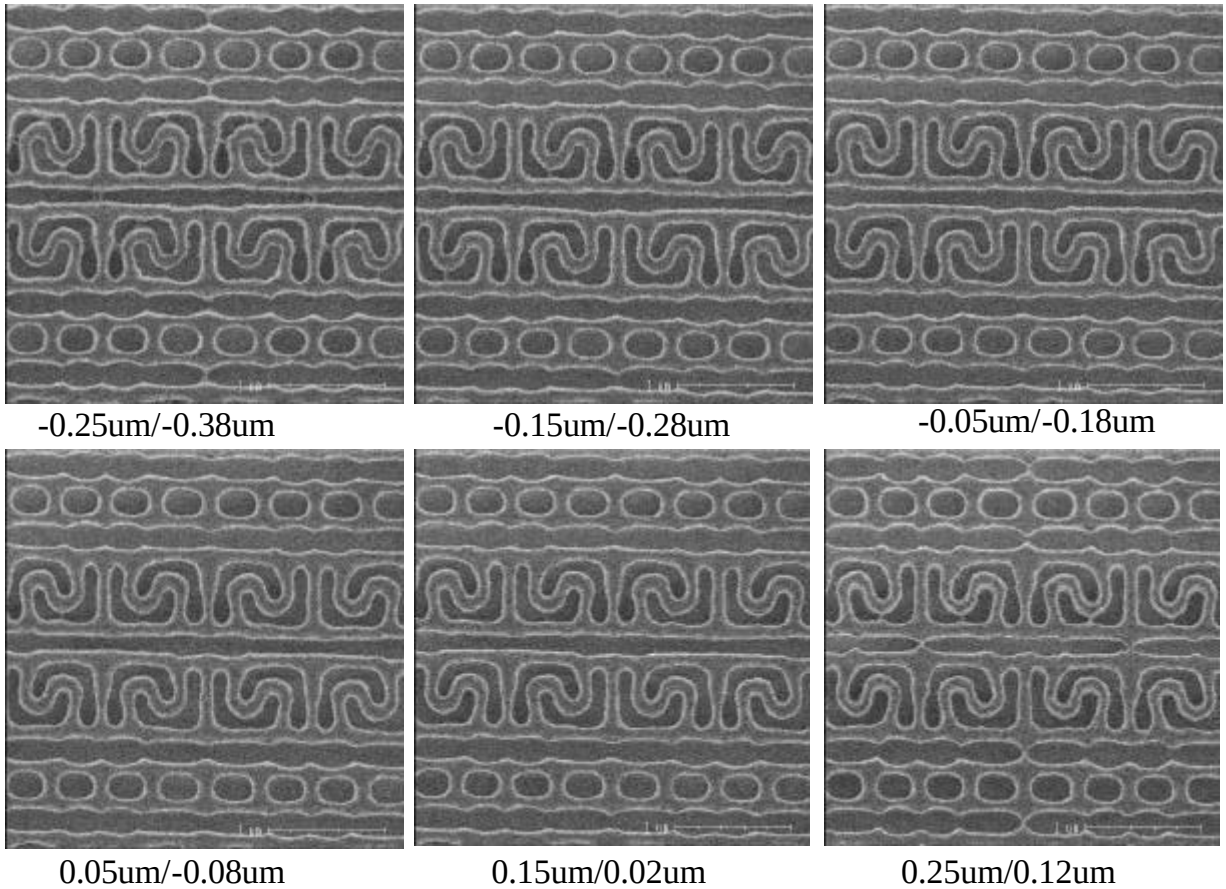

Figure 10. AltPSM in **Figure 9** patterned through PSM/trim mask focus. DOF for this design was larger than 0.40um for both PSM and trim mask focus variations.

Figure 11. AltPSM in **Figure 9** patterned with 13% dose steps.

In order to pattern the contact layer at k_1=0.35, a novel single exposure AltPSM patterning technique was developed. The novelty of this approach is based on supplementing alternating phase shifted contacts with alternating sub-resolution phase assisted subcontacts [4]. Due to particularities of contact layer patterning, no unwanted phase edges are created, thus single exposure patterning is adequate. The suggested approach is applicable not only to well-ordered memory cache, but for random logic layout as shown in **Figure 12**. **Figure 13** shows reasonable process latitude for contacts patterned with such an approach using 193nm exposure tools and resist at k_1=0.35. Excessive mask making demands and patterning concerns usually associated with the use of sub-resolution features are successfully negated in this approach, as the linear size of sub-resolution assist sub-contacts can be made as large as 0.85 of the desired drawn contact size without printing, due to a fortuitously large MEEF value of ~4 for these features.

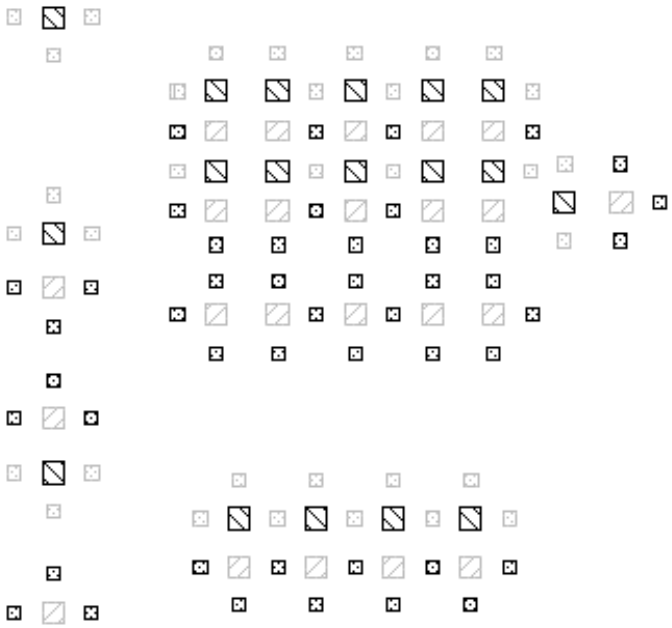

Figure 12. CON AltPSM applied to logic. Approach uses phase-shifted contacts and phase-shifted sub-resoltion square-assist features.

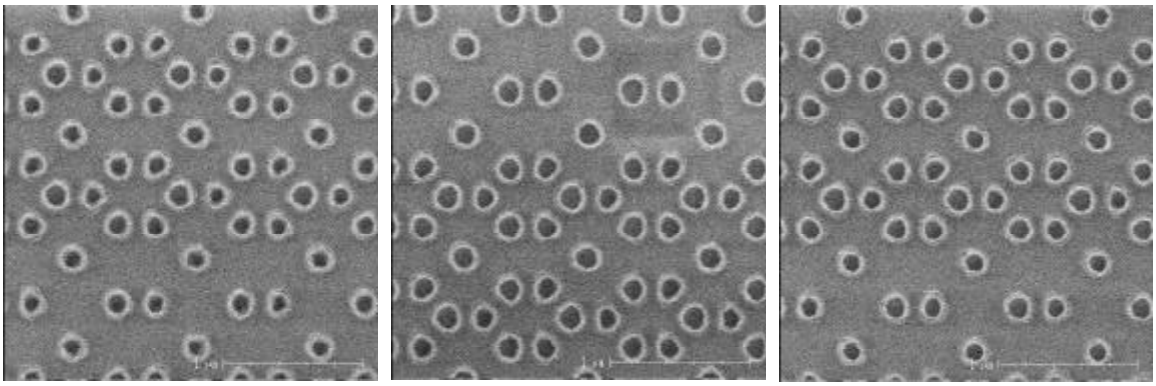

Figure 13. Patterning of AltPSM contacts with 193nm at a k_1 of 0.35 through focus steps of 0.2um.

Use of the proposed single exposure AltPSM technique provides a robust, "bridge resistant" way of patterning contacts at k_1=0.35, but it is not without its patterning drawbacks. Most noticeable is the limited ability of OPC to control contact shape near closely and non-uniformly-placed phase shifted contacts, as the MEEF value for the dark region between the contacts can go to 0. As a result, the contact shape deviates from circular for various layout configurations (**Figure 14**).

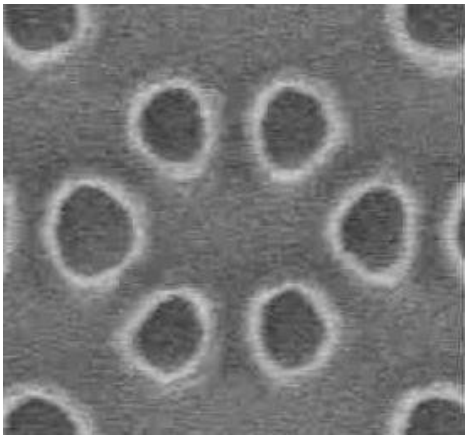

Figure 14. Noncircular contacts patterned with AltPSM. Strong destructive interference reduces the ability to shape contacts with OPC.

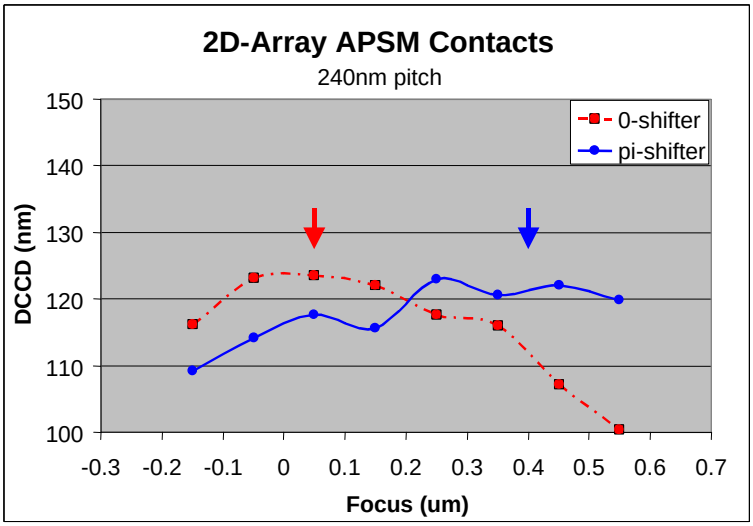

Figure 15. CD versus focus for 240nm pitched nested AltPSM contacts. Best focus for zero and 180 degree contacts are different due to 4 degree reticle phase error.

Another AltPSM contact patterning drawback is sensitivity to phase errors. In the case of gate patterning, deviations from 180º phase shift induce a lateral shift to the gate without significantly affecting gate size. In AltPSM contact patterning, however, deviations from 180º phase shift induce a separation in best focus between 0 and π shifted contacts as demonstrated in **Figure 15**. However, even in the presence of non-180º phase shift characteristic to 90nm technology, the remaining usable DOF for AltPSM contacts is still = 0.4um.

AltPSM contact patterning is also sensitive to the intensity imbalance between 0 and π phased contacts. Uncompensated intensity imbalance results in different printed contact sizes between 0 and π contacts despite having the same Cr aperture size on the reticle. Although techniques such as sidewall chrome alternating phase shift mask (SCAAM) [5], have been proposed to reduce the effect

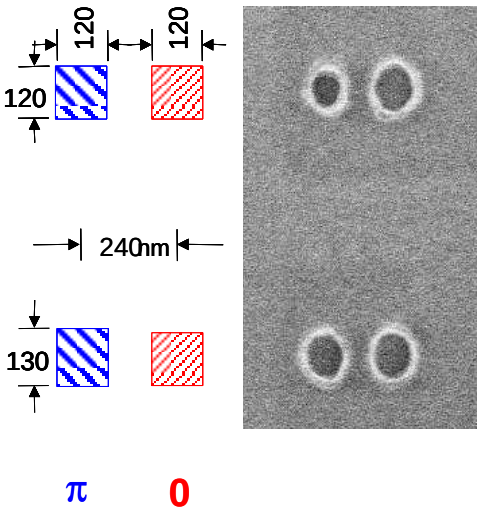

Figure 16. Differential sizing of zero and 180 degree contact pair to compensate for intensity imbalance.

of intensity imbalance, we were able to adequately correct for this affect by differentially sizing two types of contacts, a simple demonstration of which is shown in **Figure 16**.

Even though methods and synthesis tooling could be devised to pattern necessary limited types of layouts at k_1=0.35, the corresponding AltPSM mask making challenges for 193nm-based 65nm node high volume manufacturing remains significant. Production worthy phase metrology tools with in-die measurement capability are needed, as across reticle phase control needs to be better than ±3º in order not to impinge on DOF excessively. Furthermore, intensity imbalance with AltPSM may require novel AltPSM approaches and more complex OPC methods. Some of the newly proposed image intensity balancing proposals such as SCAAM or more evolutionary aperture sizing combined with chrome undercut wet etch (**Figure 17**) will be needed. Data in **Table 1** show relative benefits and drawbacks of referred compensation techniques.

glass
chrome
chrome oxide
air

		65-nm Node Performance		Mask Scalability			
		best focus	through focus	chrome lifting	mask level alignment	chrome thickness	sidewall angle
space width bias	S_0 S_{180}	+	+	+	+	+	–
undercut 1 side		+	+	–	+	+	–
undercut 2 sides		–	–	–	+	+	–
side wall chrome		+	+	+	–	–	+

Table 1. Comparison of the relative advantages and disadvantages of different alternating phase shift mask topography structures. The structures shown are cross sections through the line/space features. Good performance is denoted by "+", potential issues with performance or mask making are denoted by "-".

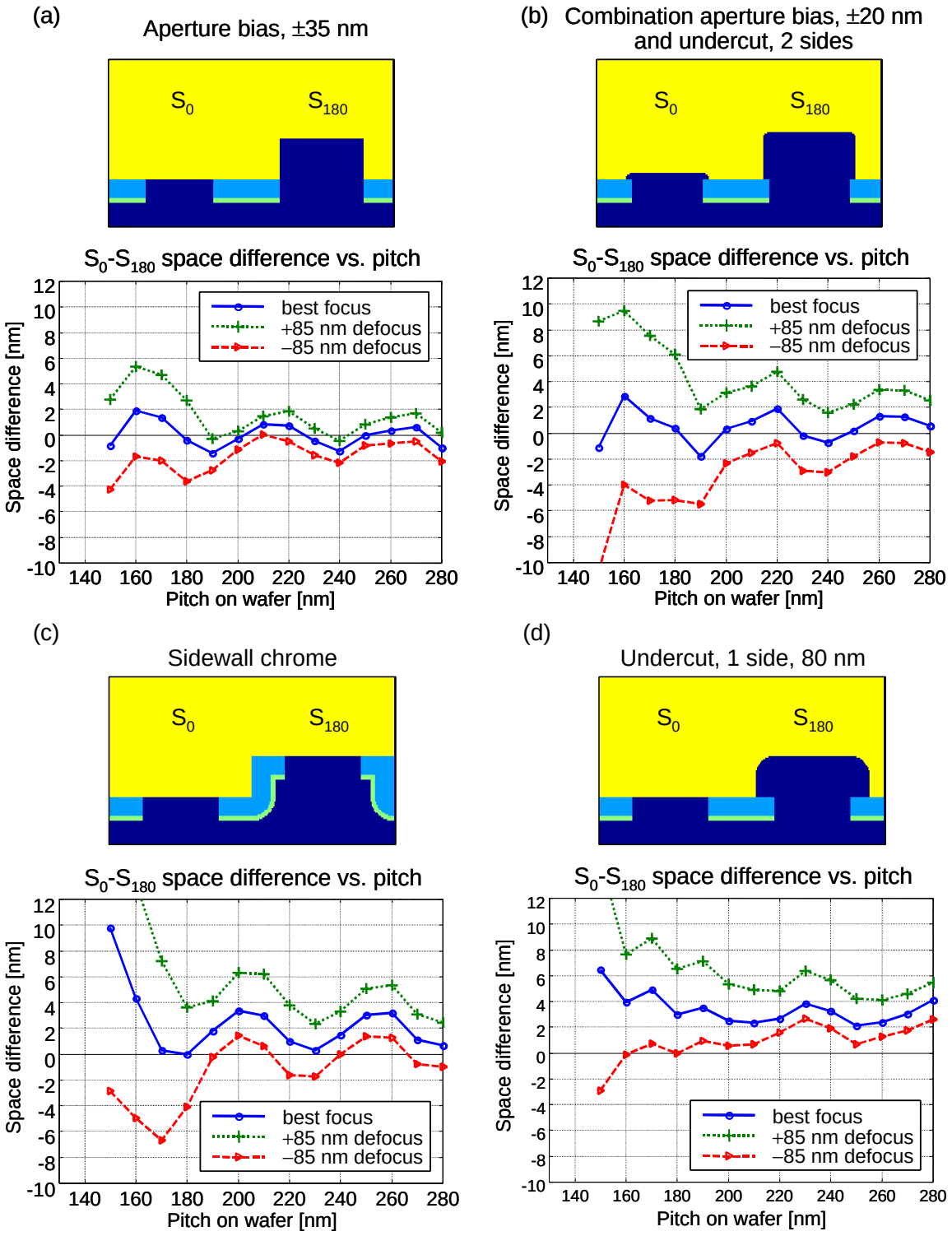

Figure 17. The difference between 0° and 180° spaces printed with different alternating phase shift mask structures using exposures at 193 nm with 0.85 NA and sigma of 0.4. The chrome linewidth on the mask is 280-nm and the pitch and focus are varied. The image imbalance has been corrected with (a) aperture biasing, (b) combination of aperture bias and chrome undercut, (c) sidewall chrome, and (d) chrome undercut on one side. The illumination is randomly polarized.

Most importantly, significant advances in mask inspection and repair tooling are needed to meet the projected k_1=0.35 AltPSM specifications required to support 193nm-based manufacturing for the 65nm node. As k_1 decreases, the relative printability of phase defects increases, thus requiring repair tool resolution and accuracy to scale faster than the primary feature size. The main challenges for AltPSM inspection include handling of multiple layers of data by the inspection tools (chrome, 0° glass, 180° glass) and achieving the desired detection sensitivity to glass defects, which have poor contrast in an inspection tool but can significantly impact the pattern on the wafer. To meet these requirements, which are necessary to ensure high quality of the mask and wafer yields, new inspection data handling capabilities and significant improvements in the defect sensitivity of the mask inspection tools are needed. **Figure 18** illustrates the projected gap between AltPSM inspection capabilities and requirements for the 90nm node. At the current rate of inspection tool development, the inspection gap will become even larger for the 65nm node.

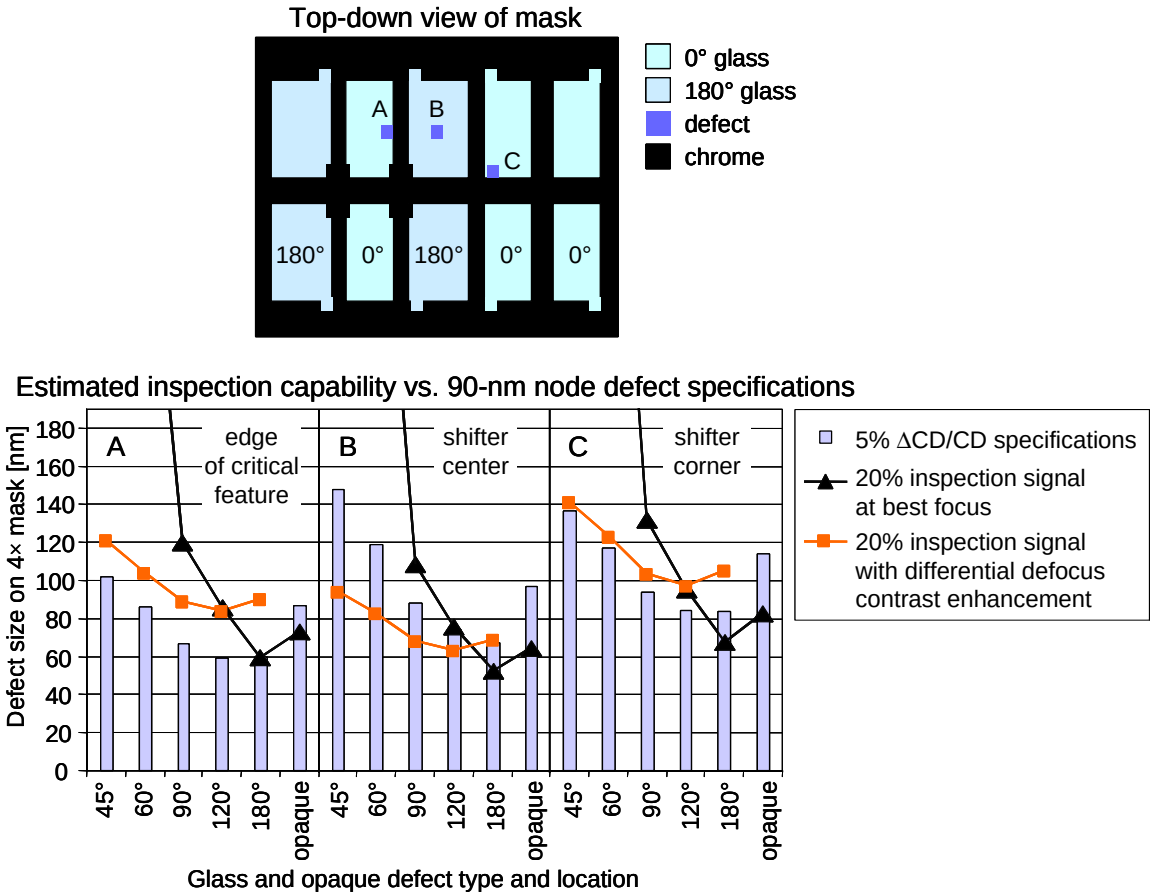

Figure 18. Estimated inspection capability vs. 90-nm node defect specifications. Comparison of the inspection sensitivity to AltPSM defects estimated from simulated aerial images of the defects and the defect specification requirements based on simulations of the poly gate layer patterning with AltPSM at 193 nm with 0.75 NA. The inspection tool is assumed to operate at a wavelength of 257nm, NA of 0.7, and σ of 0.5. For inspection, the best focus signal represents extension of existing tool capability and the contrast enhancement signal requires substantial modifications to the basic hardware of the existing tools. The comparison is given for several types and locations of glass and chrome defects.

Given the severe challenges and unsatisfactory pace of development of AltPSM maskmaking infrastructure in the past, worldwide collaborative efforts are required to support the development of AltPSM photomask technology in a cost effective and timely manner in order to enable 65nm technology node HVM.

General 65nm Node Maskmaking Challanges

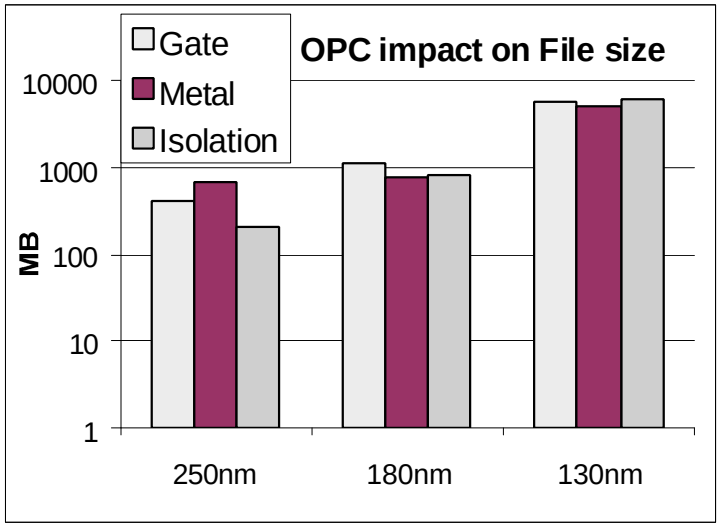

Figure 19. Technology dependence of post-OPC pattern file size for three critical layers.

Increased reliance on OPC to compensate not only for optical proximity effects but for overall lack of process latitude has led to the use of advanced OPC on more masking layers than one would expect from purely optical proximity compensation considerations. Large and fast changing MEEFs associated with complex OPC structures necessitate the use of corrections on the smallest possible grid available, which in turn cause data prep, tapeout, mask write and inspection cycle times to increase explosively. **Figure 19** shows that, due primarily to OPC, the volume of pattern data is growing much faster than the circuit density is increasing. In addition, as we shrink processes, it is necessary to apply OPC to upper metal and implant layers that formerly did not need it. Two sorts of problems arise from the growth of pattern data. The most serious occur when we exceed limits of hardware or software inside the equipment we use to write or inspect masks. The time required to diagnose these problems and upgrade the affected equipment adds directly to the time needed to introduce new products. The second type of problem associated with expanding data is the cost of computation needed to apply OPC and perform the other steps necessary to tape designs out. AltPSM is another relatively recent development that adds to the computing burden, although it contributes far less to data volume expansion than OPC.

Others have proposed methods to constrain the expansion of data due to OPC [6]. We welcome such developments, but we realize that they can only slow the expansion that we face. Increasing pattern complexity is inevitable, so we must look for other ways to reduce the cost of computation. An obvious and common approach is to exploit redundancy in hierarchical designs. This is most useful for tapeout steps preceding OPC. After OPC, much of the redundancy is lost because OPC solutions for identical cells differ if we place them in different surroundings. In addition to exploiting hierarchical redundancy, we must therefore develop faster and less expensive methods to process relatively flat pattern data. We also want the computing architecture to be scalable and flexible. Distributed computing fits these requirements nicely, and a recent report shows that it is very effective for certain tapeout steps [7].

Compressing pattern data with standard methods such as Lempel-Ziv or Huffman coding would not help to solve the computational failures and expenses we associate with data volume expansion. On the other hand, some improvements to stream data formats now being considered by SELETE and SEMI working groups, such as compact representations of polygons and arrays, could increase computational efficiency in addition to reducing the size of stream files. Ideally, organization of pattern data should make it easier to apply the distributed computing methods that we prefer to use with large designs. The motivation for our interest in new hierarchical stream formats is to reduce cost of computation, not to feed such data directly into mask writers and inspection systems. Computation already embedded within such hardware is generally the least flexible and most difficult to scale with larger pattern files, and limited ability to verify output raises concerns about quality. Combined use of APSM and aggressive OPC could lead to even greater data volume explosion requiring even faster acceleration of resolving this issue.

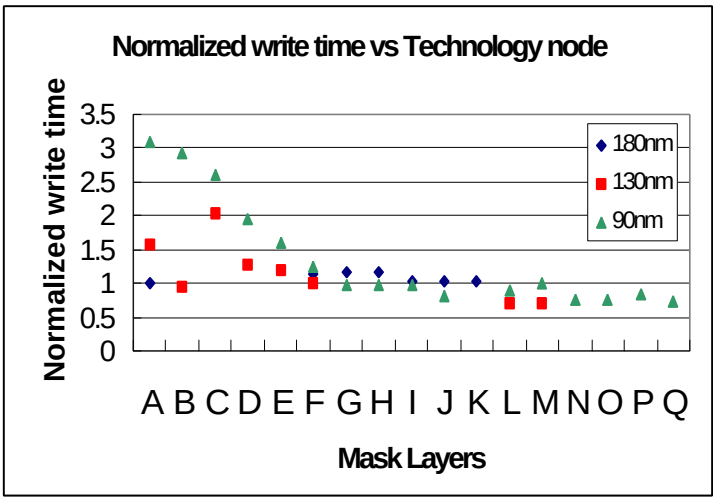

Figure 20. Write-time increase vs. technology node.

The complexity of advanced OPC design demands the acceleration of developing mask writing, defect inspection equipment, repair tools, and CD metrology tools with database pattern recognition capability. Data volume explosion and write time increase are approaching to an unaffordable regime as shown in **Figure 19** and **Figure 20**. Advanced mask repair techniques have been developed to save the expensive and precious OPC and phase shift masks to reduce the mask cost. This will become a routine practice for future mask manufacturing rather than an engineering practice. **Figure 21** shows the reconstruction of OPC features and EPSM contacts. Extreme mask making dimensional control requirements imposed by wafer patterning technology requirements and ever increasing MEEFs require similarly substantial advances in mask making metrology capabilities. Current CD-SEM measurement precision is greater than 3nm, about 3 times larger than the estimated random CD error components of the e-beam writer alone. Substrate charging is the fundamental limiter of extending CD-SEM metrology needed for meeting mask making CD control requirements. Development of novel mask making specific non-SEM metrology and tooling in time for 65nm Technology node development and manufacturing might be required.

Conclusions

The 65nm technology node high volume manufacturing will start on schedule in 2005. Initial process development in 2002-2003 will have to be supported with 193nm tooling and material that will present severe challenges to all areas of mask making infrastructure and process development because of the stringent requirements for strong phase shifted masks coupled with advanced OPC. Advent of 157nm technology in 2003 and 2004 will pose its unique challenges to mask making mainly in the particle protection area. It is clear that collaboration between all the stakeholders is required in order to meet, on time, the challenges of 65nm node.

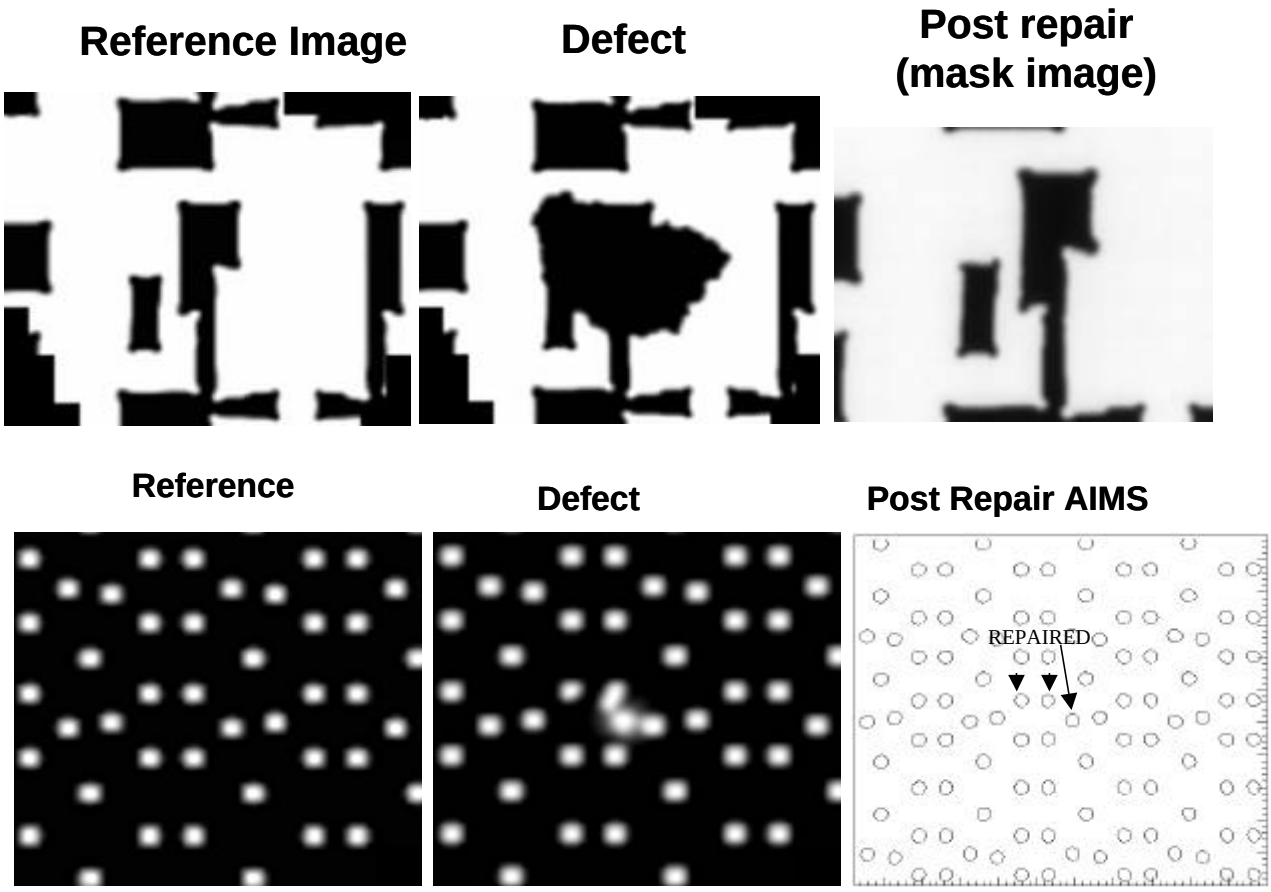

Figure 21. Repair results on mask with OPC and EPSM contact mask.

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